PHO-TR331

CONVERSION OF DIGITAL TELEVISION DISPLAY SYSTEM TO 729/525 SYSTEM

CONTRACT NAS 9-1261

29 SEPTEMBER 1967

PREPARED FOR

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

MANNED SPACECRAFT CENTER

PHILCO-FORD CORPORATION

Philco Houston Operations
WDL Division

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Houston, Texas

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FOREWORD

This report was prepared by Philco Houston Operations in response to MOSL Task Order No. 049a, entitled "729/525 Conversion of Digital Television Display System".

The Task Order was authorized under Part II Paragraph 2 of the Statement of Work to Modification No. 47 to Contract NAS 9-1261.

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SECTION 1

INTRODUCTION

1.1 GENERAL

This report was prepared in coordination with, and under the direction of, the Information Systems Division (ISD), Data Systems Development Engineering Staff. The effort completed on this task and subsequently reported in this document encompasses the investigation and definition of methods for providing 525 lines-per-frame video from the ISD evaluation prototype, Digital Television Display System (DTDS).

Several approaches for providing DTDS 525 video were investigated to establish feasibility, extent of existing hardware and program changes needed, and overall cost. The results of these investigations are recorded herein.

SECTION 2

OPERATIONAL ANALYSIS OF THE 729/525 DIGITAL TELEVISION DISPLAY SYSTEM

2.1 GENERAL

With any high resolution digital TV system having a line rate greater than 525 lines per frame (for example 729 or 945 lines/frame), a need may exist to distribute this TV data to remote stations over standard 525-line video channels.

If the digital TV data rate is greater than the bandwidth of the carrier and receiving equipment, a reduction in this data rate must be made to make it compatible with this equipment. When this reduction is made, the amount of video data that can be transmitted is proportionally reduced.

2.2 COMPUTER/DTDS OPERATION

Due to the previously-stated decreased data rate, the amount of information that can be presented on any given display will be reduced, and thus the programming of displays in 525-line TV data must be restricted. Considering the restrictions in light of the different methods possible for the conversion, there is an analog conversion method (double-ended storage tubes, 525 camera focused on a 729 monitor, etc.) with the restriction of limiting or avoiding the use of the smaller size characters. In the digital methods outlined in this report there is also a restriction on the amount of data bits per line and the number of lines available for data display.

Specifically, for 525-line operation the restrictions would be placed on the addressing of the data as follows:

$$0 \leq X \leq 576$$
$$0 \leq Y \leq 480$$

(Display Language Coordinates)

or

$$0 \leq X \leq 866$$
$$0 \leq Y \leq 768$$

(Computer Language Coordinates)

These correspond to the present DTDS address limitations of

$$0 \leq X \leq 832$$
$$0 \leq Y \leq 640 \qquad \text{(DL Coordinates)}$$

or

$$0 \leq X \leq 1024$$
$$0 \leq Y \leq 1024 \qquad \text{(CL Coordinates)}$$

As will be illustrated in Paragraph 3.3.2.3, this addressing range could be moved. For example, X could range over an area given by $256 \leq X \leq 832$ (DL Coordinates), and Y could be specified by $128 \leq Y \leq 608$ (DL Coordinates).

Since no analog methods of conversion were investigated in this task, no evaluation between the two restrictions mentioned above was conducted. Also, no investigations were made into the present computer programs to determine the magnitude of the changes necessary to meet the above restrictions.

2.3 CONSOLE OPERATIONAL PROCEDURES

The restrictions on the operation of the DTDS (525 mode) from the consoles would be the same as those mentioned in Subsection 2.2. These restrictions are upon the addressing of display data that can be entered via console thumbwheels or trackball. For examble, when typing from the keypack, a Margin or Carriage Return would have to be initiated on or before an X-address of 576 (DL Coordinate) was reached. Likewise, the Y-addressing would have to be between 0 and 480. This criteria would hold for vector generation and data generated by the trackball in continuous mode.

2.4 USE OF RANDOM ACCESS MEMORY (RAM) BACKGROUNDS

The 729 DL backgrounds stored on the DL RAM will also suffer loss of information. As mentioned in the previous paragraphs, data not in the addressing ranges for 525-line data will be lost. Either specific 525-line DL backgrounds will have to be generated, or backgrounds on which the loss of the right and upper portions are immaterial will have to be used.

SECTION 3

FUNCTIONAL ANALYSIS OF THE 729/525 DIGITAL TELEVISION DISPLAY SYSTEM

3.1 GENERAL

In the investigation of possible ways of providing a 525-line video channel from the DTDS, the following guidelines were used.

A. A digital conversion method in order to retain the inherent video quality of a digital TV system.

B. Minimum DTDS downtime for implementation.

C. 525-line video with a bandwidth comparable to commercial video.

D. Minimization of changes to the operational procedures.

E. Minimum cost.

F. Retention of 729-line capability.

Although not all methods considered in the investigation are mentioned in this report, it is felt that the four methods outlined in this report best follow these guidelines.

- Method I - Requires addition of a 525-line refresh memory
- Method II - Requires addition of a 525-line refresh memory and major modification to DTDS
- Method III - Converts a 729-line refresh memory to a 525-line refresh memory
- Method IV - Requires a core buffer memory

3.2 MODIFICATIONS AND/OR ADDITIONS NECESSARY FOR ANY METHOD

3.2.1 Sync and Timing

A basic oscillator for generating 525-line video sync and timing must be added. The basic oscillator frequency is dependent upon the raster line standard and the total bits per horizontal video line. Assuming 704 bits per line with a 525-line standard, the basic frequency becomes:

(525 lines/frame) (704 bits/line) (30 frames/sec) = 11.088 MHz

From this frequency, the following signals are required:

- TV Composite Sync
- TV Vertical Drive
- TV Horizontal Drive
- TV Blanking.

All system clocks are also derived from the same oscillator. They include:

- Serializer Shift Clock (1/2 basic frequency)
- System Clocks (2.772 MHz, 1.386 MHz, etc.).

3.2.2 DTDS 525 Video Considerations

The TV monitors utilizing cathode ray tubes (CRT's) in a raster-type digital television display system are driven by a digital video data stream and by synchronous control signals.

3.2.2.1 Video Control Signals

The video control signals required by a raster-type digital TV monitor are horizontal deflection controls (sync or drive), vertical deflection controls (sync or drive), and blanking.

3.2.2.2 Deflection and Blanking Controls

Synchronizing pulses must be supplied to the monitor vertical and horizontal oscillators. These pulses position the video raster on the CRT screen by controlling the frequency of the deflection circuits that cause the vertical and horizontal scanning.

Blanking pulses are part of the video information stream. They obliterate the retrace lines by changing the signal to the black level during the time the scanning circuits produce retraces. The vertical blanking pulses have the function of eliminating the retrace lines produced when the electron beam is deflected from bottom to top in each field. Vertical blanking is 1.472 milliseconds (msec) at the end of Field 1 and 1.408 msec at the end of Field 2.

Horizontal blanking pulses are used to eliminate the retrace from right to left at the end of each horizontal scan line. To express horizontal blanking as a percentage of monitor trace time, the interval between successive scan lines is defined as H. Horizontal blanking is then defined as .18H or 11.5 microseconds (μsec). Refer to Table 3-1 and Figures 3-1 and 3-2 for more detailed video signal characteristics.

3.3 METHOD I

Method I would entail the addition of a 525 Mode cycle to the existing DTDS routines. This 525 Mode cycle would start after a 729 routine has sent CL and Field 2 (F2) DL to a 729 recirculator memory (RM). The 525 cycle would recall, to the assembly core memory (ACM), Field 1 (F1) from the 729 RM, then transfer a portion of it to the 525 RM. It would then recall F2 DL from the 72 RM and transfer the corresponding portion of it to the 525 RM. (Refer to Figures 3-3 through 3-5 for basic block diagrams.)

3.3.1 Operational Requirements

The DTDS will operate as at present with one exception: when Method I (MI) 525 Mode is selected, a 525 Mode cycle will be included in all routines that generate DL for that channel selected. Some of the MI 525 Mode operations are briefly outlined in the following. (Refer to Philco Houston Operations (PHO) Specification SS-05496, Paragraphs 3.5.4.3.1 through 3.5.4.3.13, for further details.)

TABLE 3-1

DTDS VIDEO CHARACTERISTICS

	729 LINE PROCESSOR	525 LINE PROCESSOR
LINE FREQUENCY	21,870 LINES/SECOND	15,750 LINES/SECOND
FIELD RATE	60/SECOND	60 PER SECOND
FRAME RATE	30/SECOND	30 PER SECOND
INTERLACE	2:1	2:1
LINES PER FIELD	364.5	262.5
TOTAL HORIZONTAL ELEMENTS	1024 BITS/LINE	704 BITS/LINE
VISIBLE HORIZONTAL ELEMENTS	832 BITS/LINE	576 BITS/LINE
TOTAL VERTICAL ELEMENTS	729 LINES/FRAME	525 LINES/FRAME
VISIBLE VERTICAL ELEMENTS	640 LINES/FRAME	480 LINES/FRAME
TOTAL ELEMENTS	746,496 BITS	369,600 BITS
TOTAL VISIBLE ELEMENTS	532,480 BITS	276,480 BITS
HORIZONTAL SCAN FREQUENCY	21,870 LINES/ SECOND	15,750 LINES/SECOND
HORIZONTAL SCAN PERIOD	45.725 µSEC/LINE	63.492 µSEC/LINE
VISIBLE HORIZONTAL SCAN PERIOD	37.175 µSEC/LINE	51.948 µSEC/LINE
HORIZONTAL BLANKING	8.55 µSEC/LINE	11.544 µSEC/LINE
VERTICAL BLANKING	2068.003 µSEC (END FIELD 1) 2022.279 µSEC (END FIELD 2)	1471.860 µSEC (END FIELD 1) 1408.368 µSEC (END FIELD 2)

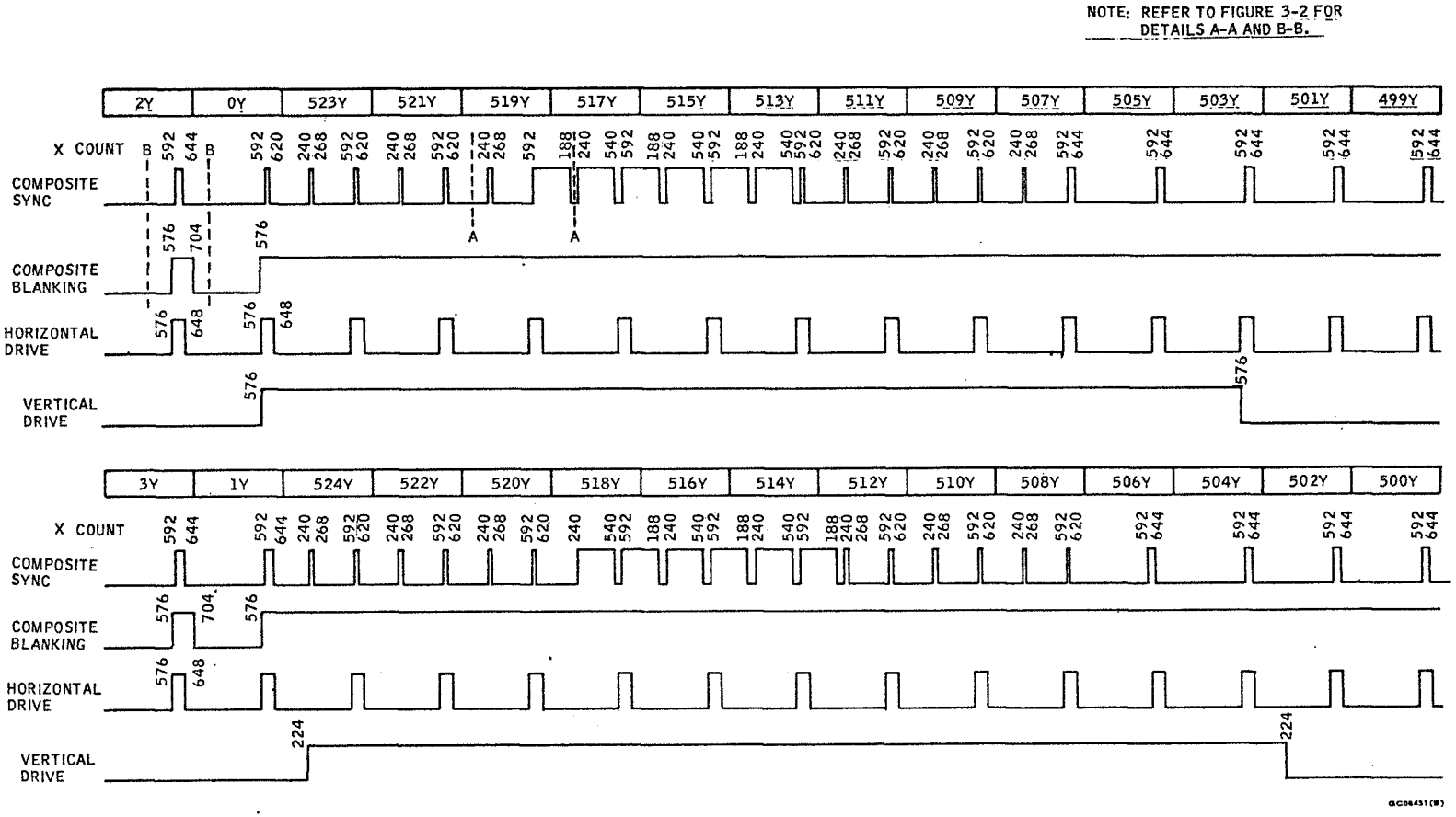


Figure 3-1 525 Sync and Timing Diagram

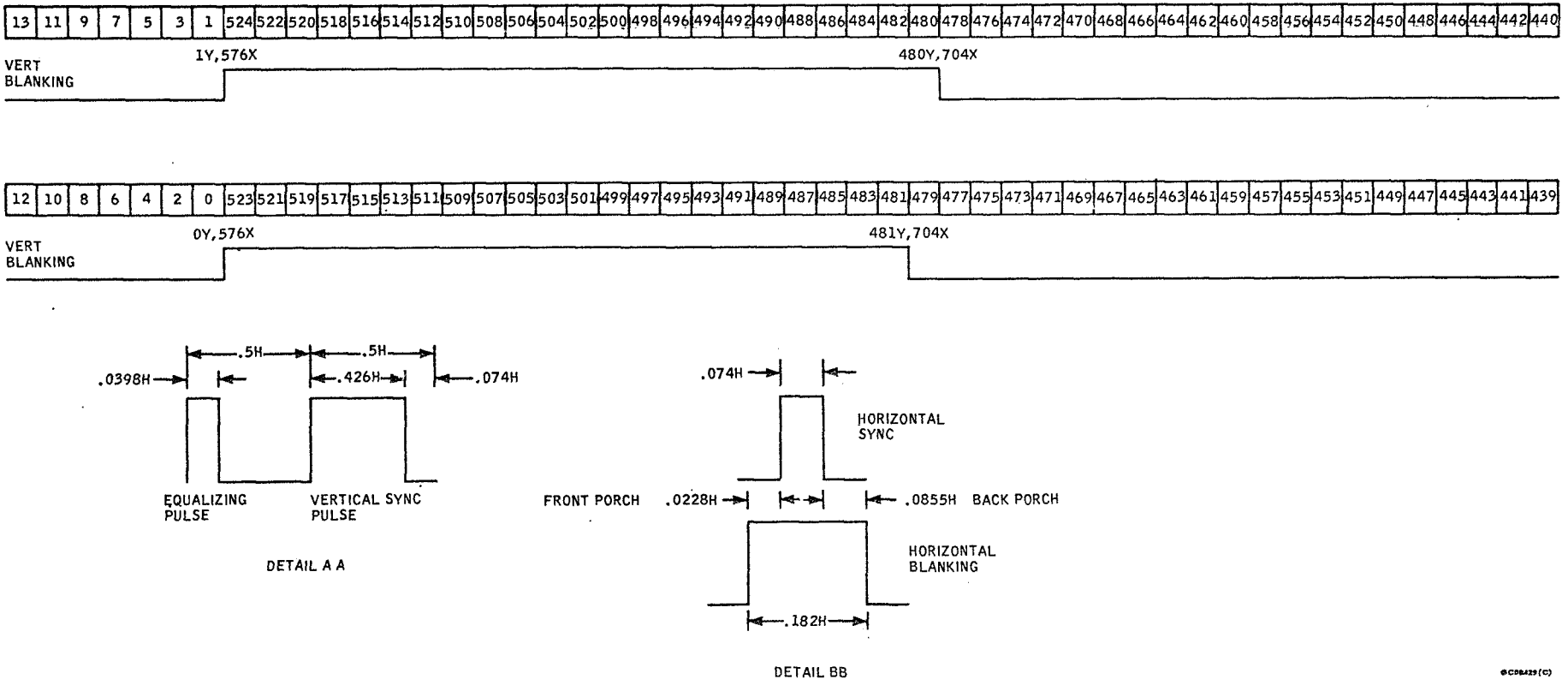


Figure 3-2 Vertical Blanking

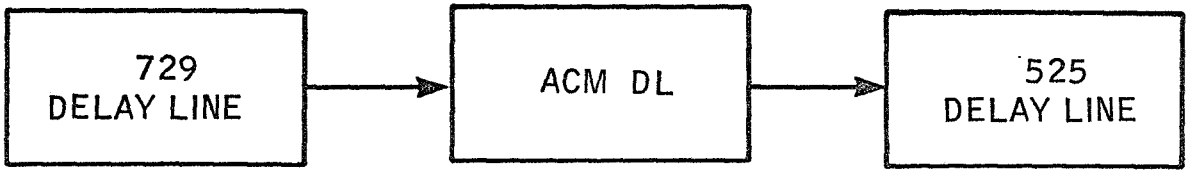


Figure 3-3 Method I Basic Concept

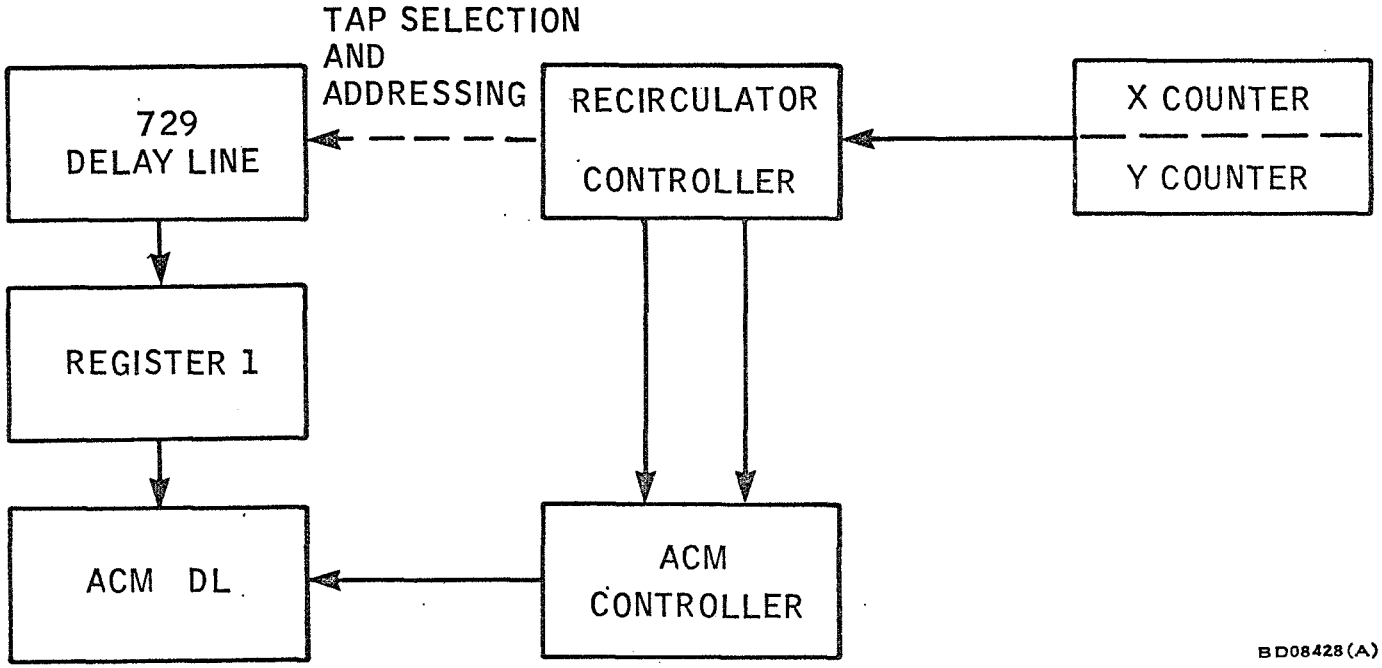


Figure 3-4 Method I 729 Recall DL

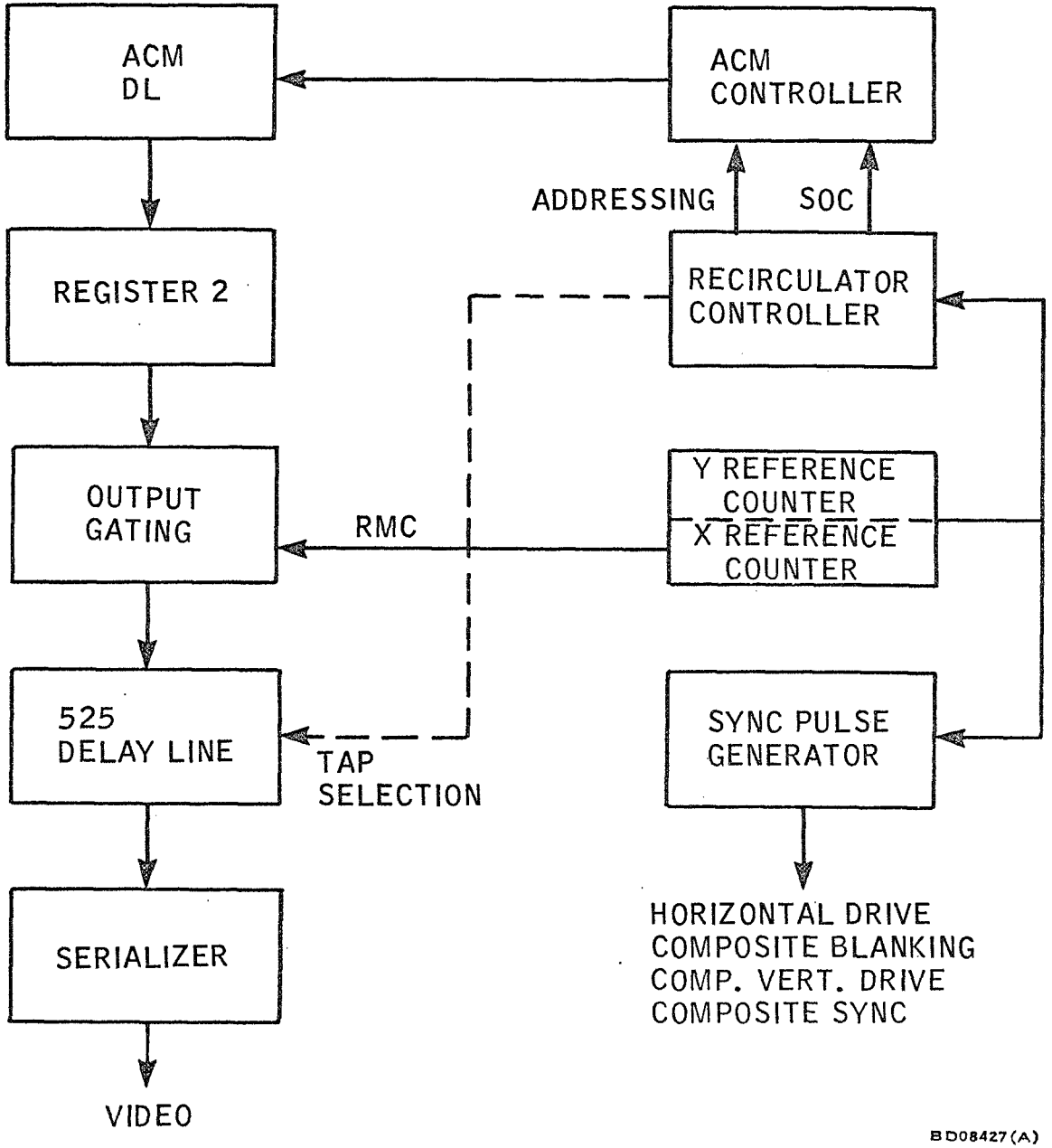


Figure 3-5 Method I 525 Write DL

A. Computer-Generated New or Updated Black and White Displays. Figures 3-6 and 3-7 show the major cycles that shall be required to generate computer-transmitted new or update B&W displays in MI 525 Mode. As can be seen from the figures, it will take 66 2/3 msec longer to complete either of these operations.

B. Other Generated Displays. In all the ways of generating displays, data is first sent to the 729 RM and is then recalled, one field at a time, to the ACM. The data is then transferred to the 525 RM.

3.3.2 Modifications and/or Additions to DTDS

The following modifications and/or additions to the DTDS components will be necessary for Method I implementation:

A. New System of Clocks

B. X and Y Reference Counters

C. Sync Pulse Generator

D. Memory Controller

   1. Addressing

   2. Write-In and Readout Pulses

E. Display Area Control

F. Recirculator Controller

   1. Tap Selection

   2. Channel Selection

   3. New Data

G. Comparator

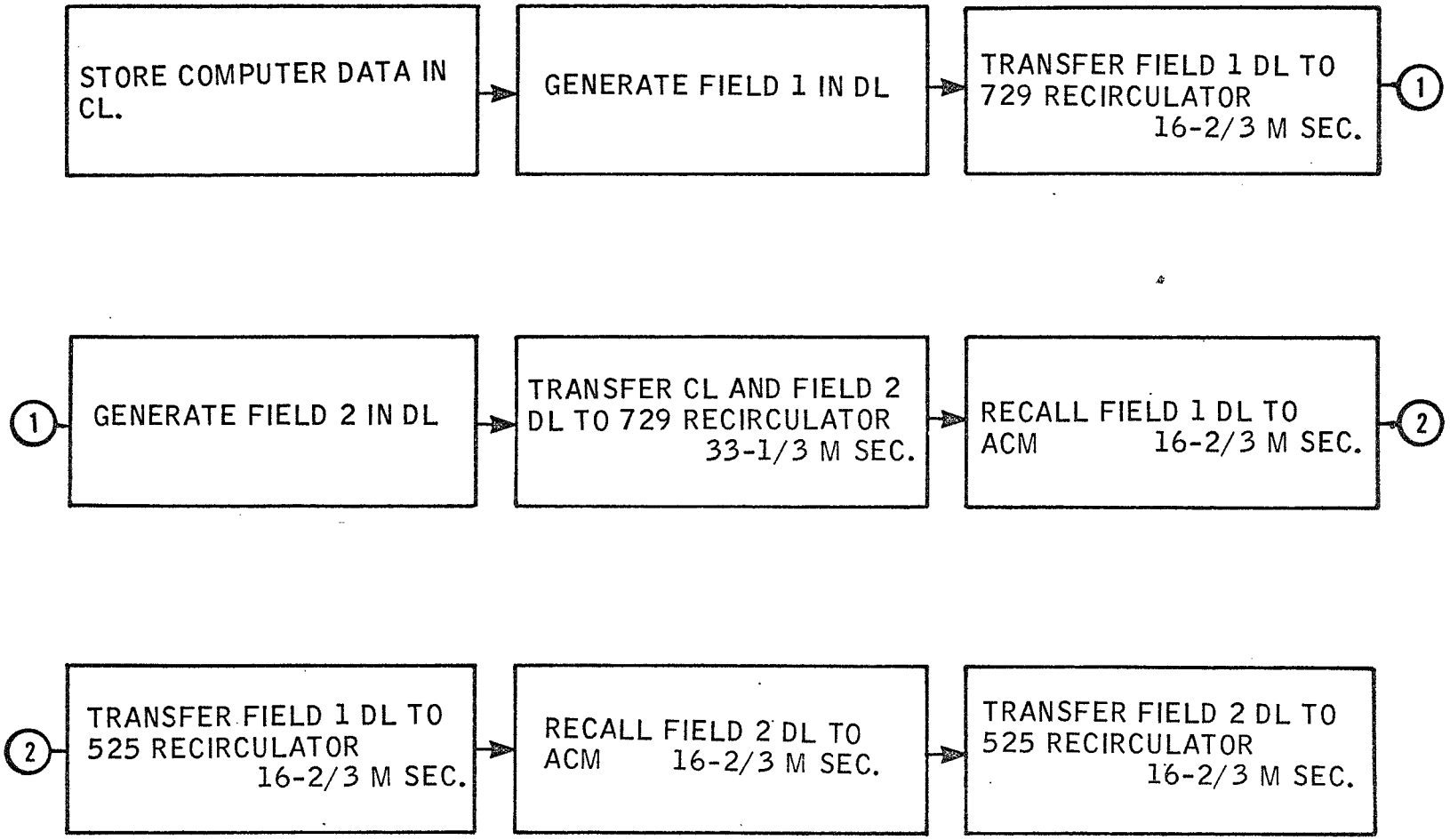


Figure 3-6 DASS B&W New Display, Method I Flow

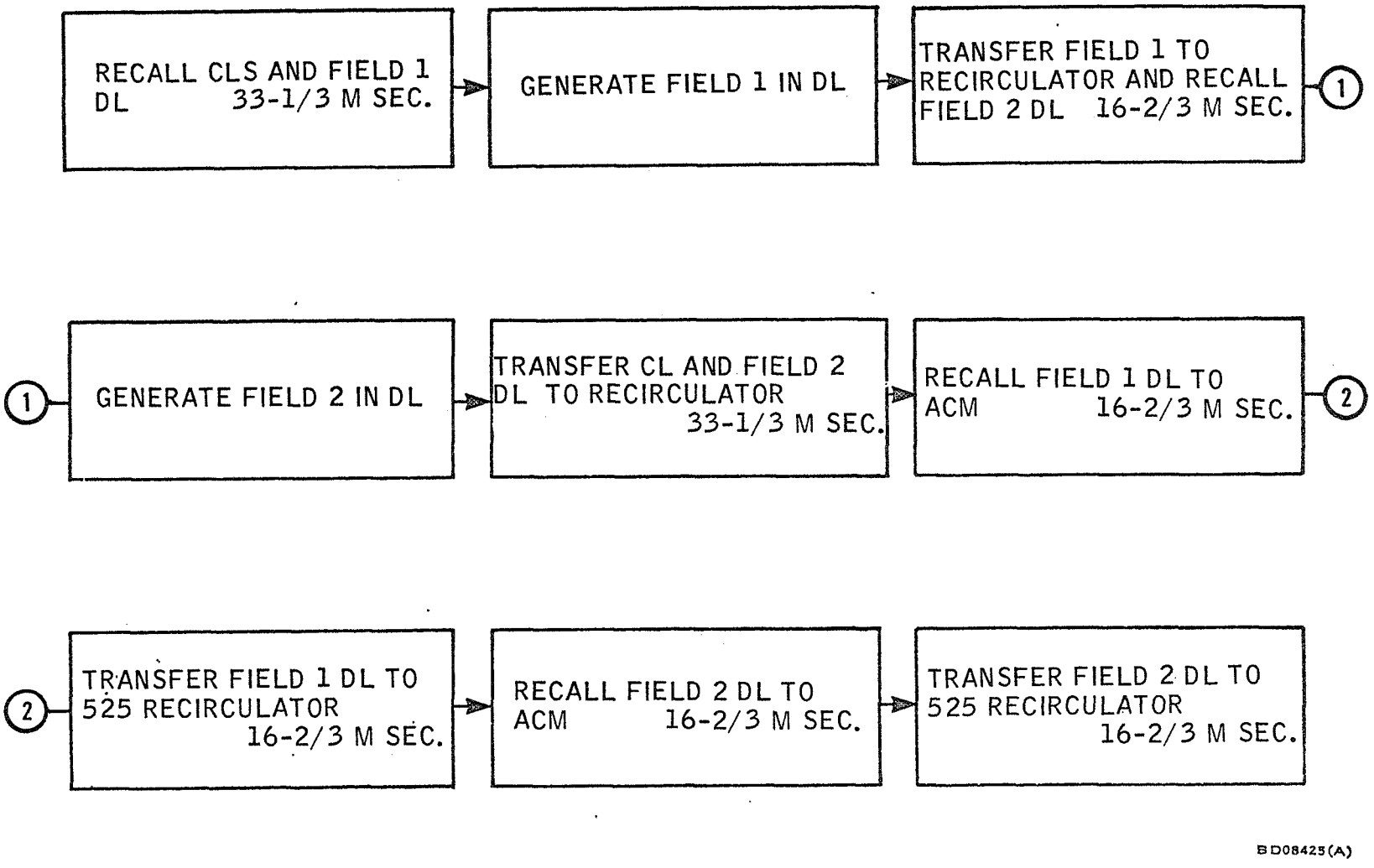


Figure 3-7 DASS B&W Update Display, Method I Flow

H. Data Output Gating

I. Serializer

J. Delay Lines

3.3.2.1 X and Y Reference Counters

The X and Y reference counters are used to furnish many of the control pulses throughout the display assembler. For example: The control pulses are used in the TV sync circuit, the ACM controller, the recirculator controller, and the output gating logic. Those changes to the reference counters are as follows:

A. X-Counters. By using the oscillator for timing, described in Paragraph 3.2.1, it is possible to pick a frequency giving a total number of bits in a raster line that is a multiple of 64. The required X-counter must count to 704 and then reset itself. This will give eleven 64-bit words per line.

In 729 operation, two X-counters are required because data is both written on, and read from, the delay lines. Method I will require only one X-counter, the X Begin Write. The counter will consist of eight flip-flops whose count will be as depicted below.

FLIP-FLOPS

X Count 4 8 16 32 64 128 256 512

The clock on the counter will be approximately 2.77 MHz, or equal to about 361 nanoseconds. The count of 512, 128, and 64 is equal to the required total of 704 bits/line. Dividing 704 by 4 yields 176 actual clock pulses. Multiplying (176) (361 nanoseconds) yields 63.5 microseconds, the required time per line for 525 operation.

B. Y-Counters. In the present DTDS the 729 Y-reference counters, End Read, Begin Write, Middle Read, are designed to count down by 2's. The Y End Read counter is used as the master counter. The counters are set up to counts 729 or 727.

Lines 729 and 728 last for one-half of a line time. (Refer to Figure 3-8 for a timing diagram.) The even-numbered lines are Field 2, and the odd numbers are Field 1.

Methods I, II, and IV will require the YMWC and the YBWC. Method III will require all four counters. The counters will operate as they do in 729 except that they will be set up to count down from smaller numbers.

3.3.2.2 ACM Controller

The ACM Controller for 729 operation contains the logic to start memory routines and detect the end of the memory cycle (see Figure 3-9). The ACM consists of two 8K 32-bit long word memories. Write routines are started by SIC signals and Read routines by SOC signals. A one clock time end cycle (NCY) signal is produced when EOC signals are received from both memories.

Signals from the sources which access the memory are *OR'ed* together and steered to set either a SIC or SOC flip-flop. Signals from the recirculator controller are *OR'ed* directly to the memory.

Figure 3-4 indicates that Method I is concerned with recalling data from a 729 channel and displaying it on a 525 monitor.

Method I will involve writing into the memory at 729 speed and reading from it at 525 speed. Thus it is necessary to control both the addressing and the Write-in and Readout rate. The memory controller for 525 will provide the following functions:

A. Addressing. The speed of addressing will be determined by which operation is active. The particular active address will be determined by which portion of the 729 picture it is desired to display. The following areas of the 729 picture can be shown in 525. (See Figures 3-10 and 3-11.) The areas shown represent a 48 percent picture loss.

B. RMSOC. The SOC pulse, which reads data from the memory, must operate at 525 speed. It must be controlled so that DL will be read out at the correct speed and at the correct time. (For example: Not in blanking.) The general pattern for pulse control in 729 is followed for 525 operation.

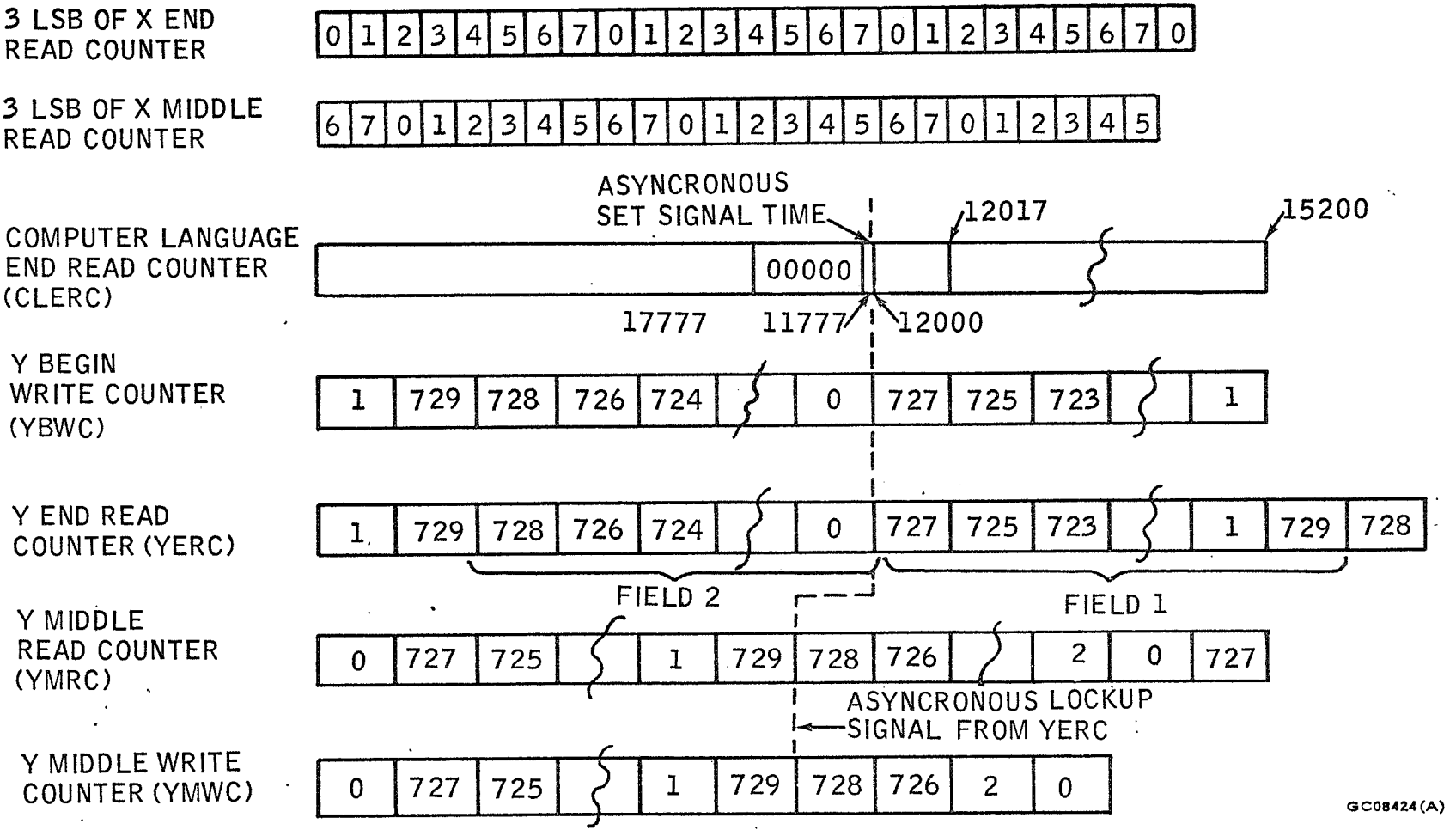


Figure 3-8 Reference Ceounter Timing Diagram

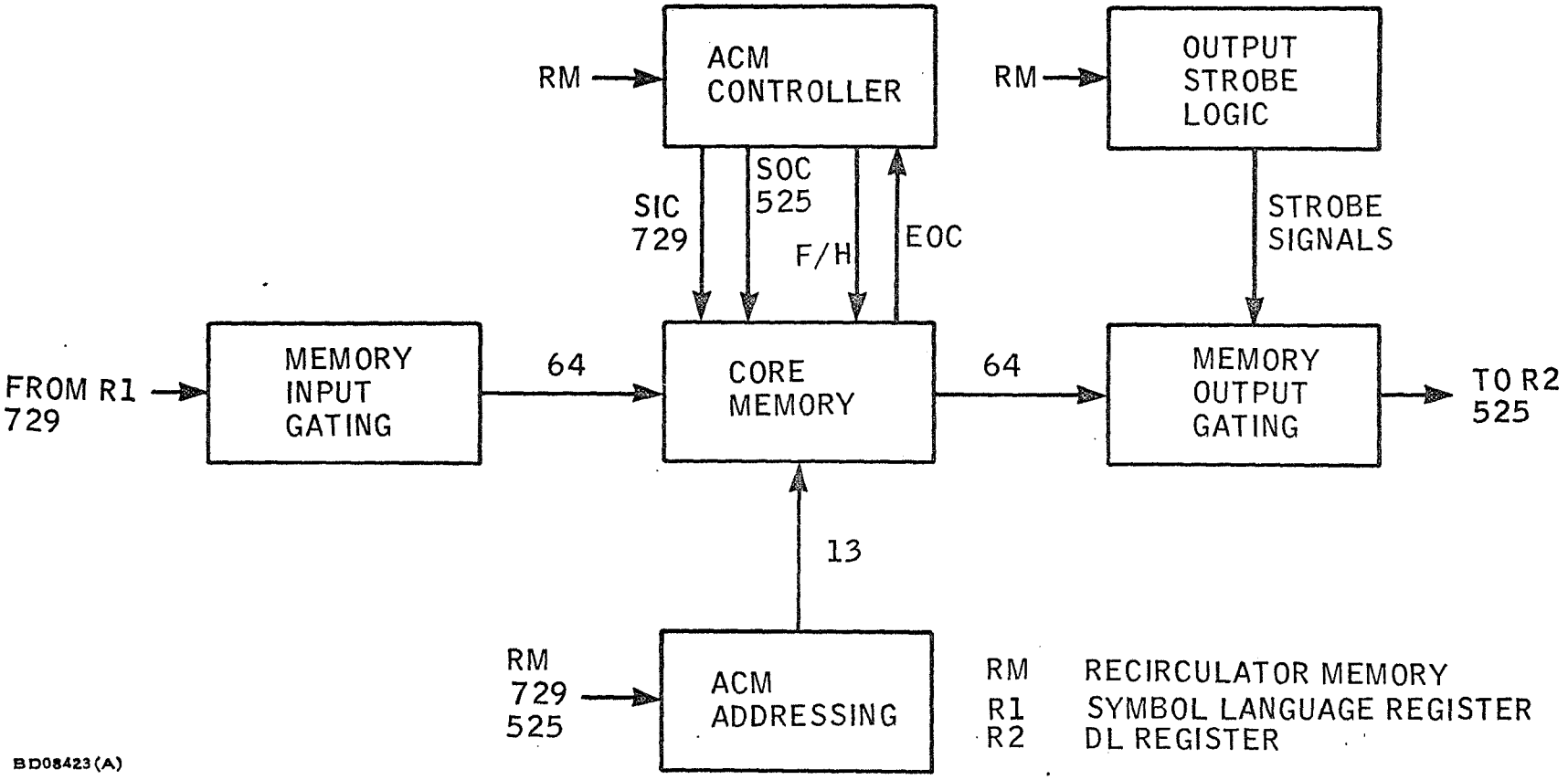
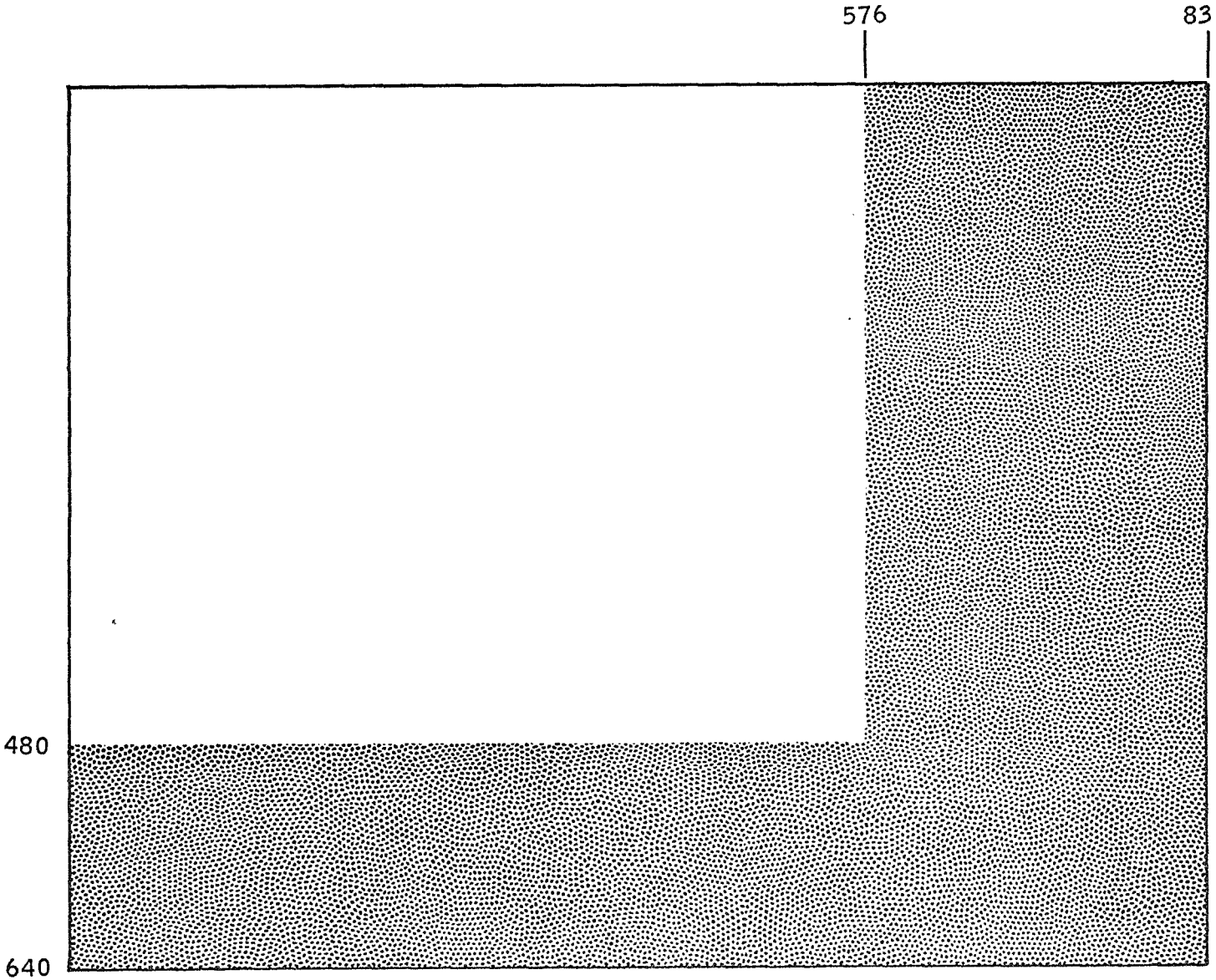


Figure 3-9 ACM Controller, Method I



NOTE 1: THE DISPLAY COULD BE MOVED TO EITHER OF THE CORNERS.
NOTE 2: 48% PICTURE LOSS.

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Figure 3-10 Corner Display, Method I Addressing

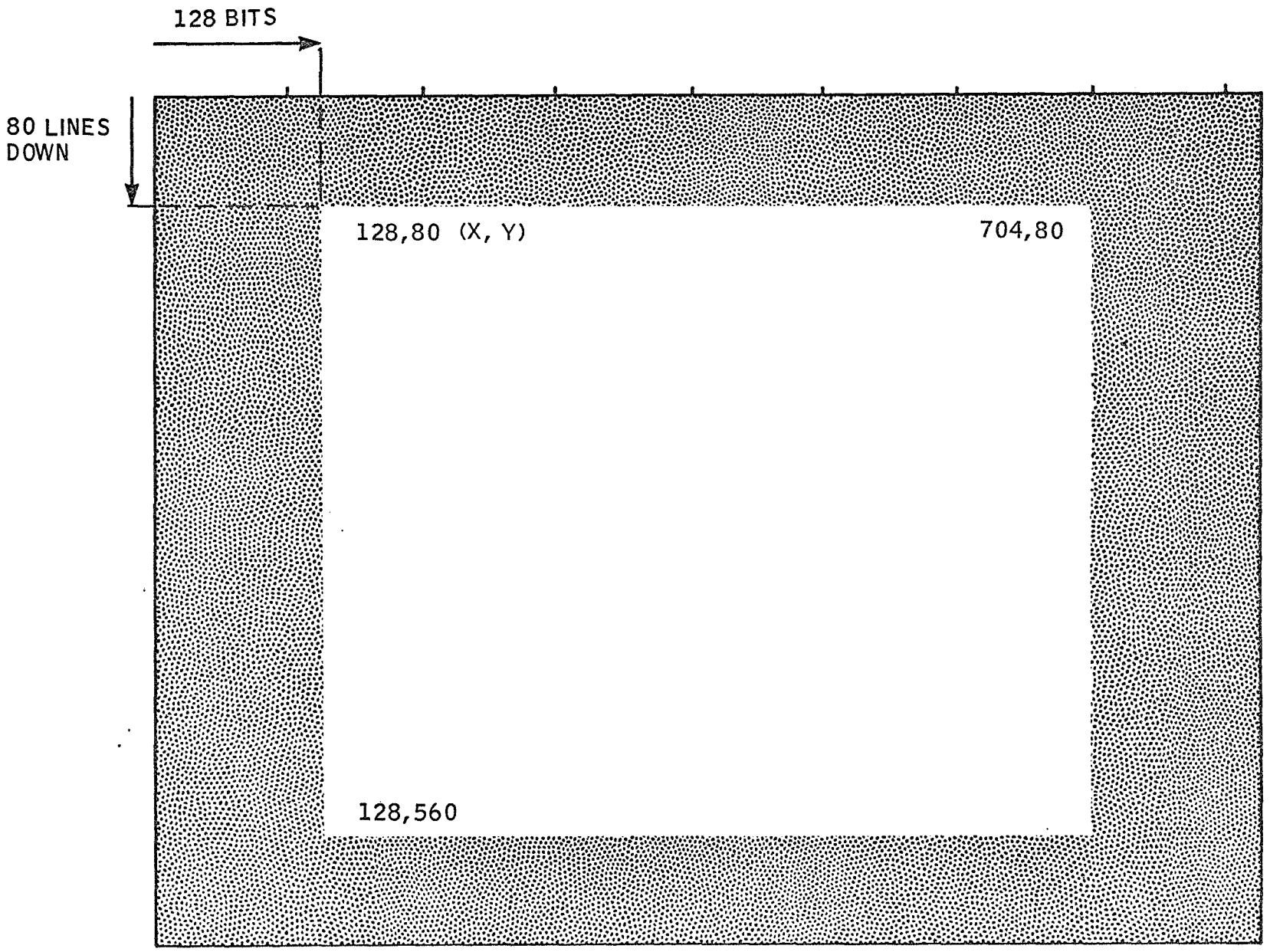

Figure 3-11 Center Display, Method I Addressing

C. RMSIC. The SIC pulse transfers data into the memory (ACM). The 729 SIC is controlled by a DLS TAP 1 or TAP 2, Read Address Enable, WXCT4, and an Enable SIC.

The Enable SIC:

- Occurs after Read Setup cycle
- Goes false at Read Complete.

The 525 SIC control will have some additions to the logic. These additions:

- Should limit to nine the number of SIC pulses generated per line
- Should limit the number of lines to a size 525 display.

This will eliminate having to clear the memory of the excess data that would be stored in a 729 field.

3.3.2.3 Display Area Control

The area of a 729 picture desired to be shown on 525 could be selected by dialing certain addresses on X and Y switches. This would allow the entire picture in 729 to be viewed in 525, although not at the same time. The entire field of 729 DL would be recalled to memory. The portion of the DL not read out for Field 1 would be left in the memory. When Field 2 DL has been read out to the delay line for 525, the data remaining in the memory would be cleared. In using this method practically no changes would have to be made in doing a recall 729 DL to memory cycle. The changes necessary for transferring data out to the 525 delay line are as follow:

- Four octal switches: One X-position, three Y-positions
- Adder
- Addressing to the computer
- Control of SIC pulses to the memory.

The X-position switch would determine how far to the right on the 729 screen the display for 525 would start. The Y-position switch would determine how far down the 525 display would start.

The adder would simply add the X and Y switch positions to the X and Y counters to determine the appropriate memory address to enable.

The readout pulse, SOC, to the memory would be controlled as described in Paragraph 3.3.2.2.

The SIC pulse would not be changed from standard 729 recall of data since the entire field must be returned to the ACM. The operational characteristics would be as follows:

- Select channel to be monitored
- Select portion of picture to be displayed
- Initiate a Read Field 1 cycle (729)
- Read complete, initiate a Write Field 1 cycle (525)
- Write complete, initiate a Read Field 2 cycle (729)
- Read complete, initiate a Write Field 2 cycle (525)
- Write complete, initiate a Memory Clear cycle
- Return system to 729 operation.

3.3.2.4 Recirculator Controller

The recirculator controller in use in the DTDS receives data and control signals from the ACM controller, central control, the grafacon controller, and the display assembler control panel. The recirculator controller controls the flow of both display language and computer language between the ACM and a selected delay line. Signals for video synchronization are also provided by the controller.

The particular channel to be written on or read from is selected by either the Write or Read Address Enable and Channel Select logic. The routine to be performed is determined by recirculator control lines receiving data from central control. The case selection logic and the setup logic decode the control signals. The setup logic establishes a starting address in the comparator control logic. The X and Y reference counters provide pulses to the Read and Write counter decodes, the Read and Write comparators, the blanking decodes, the address output gates, and the necessary signals to drive the TV.

For Method I, 525 operation, the block diagram (Figures 3-12 and 3-13) of the recirculator control is divided into a Read section and a Write section. The Read section will operate at 729 speed while the Write section will operate at 525 speed. The addition of a 525 channel selection switch is the major change in the recirculator controller Read cycle. An additional controller will have to be designed for the Write cycle, which would be at 525 speed. The sequences and operations are as follows:

A. Sequence for a Read Cycle (729)

1. Wait for ROUT COMP. Prevent Central Controller from resetting.

2. Initialize a special Read Initiate Pulse to 729 recirculator controller.

3. Set Read Busy FF and Read Lockout FF. Recall Field 1 data.

4. Set Read Setup FF.

5. Set Tap Selection FF.

6. Set Read Enable FF.

7. Reset Read Lockout FF, Load Read Comparator.

8. Reset Read Setup FF.

9. Set enable SIC FF.

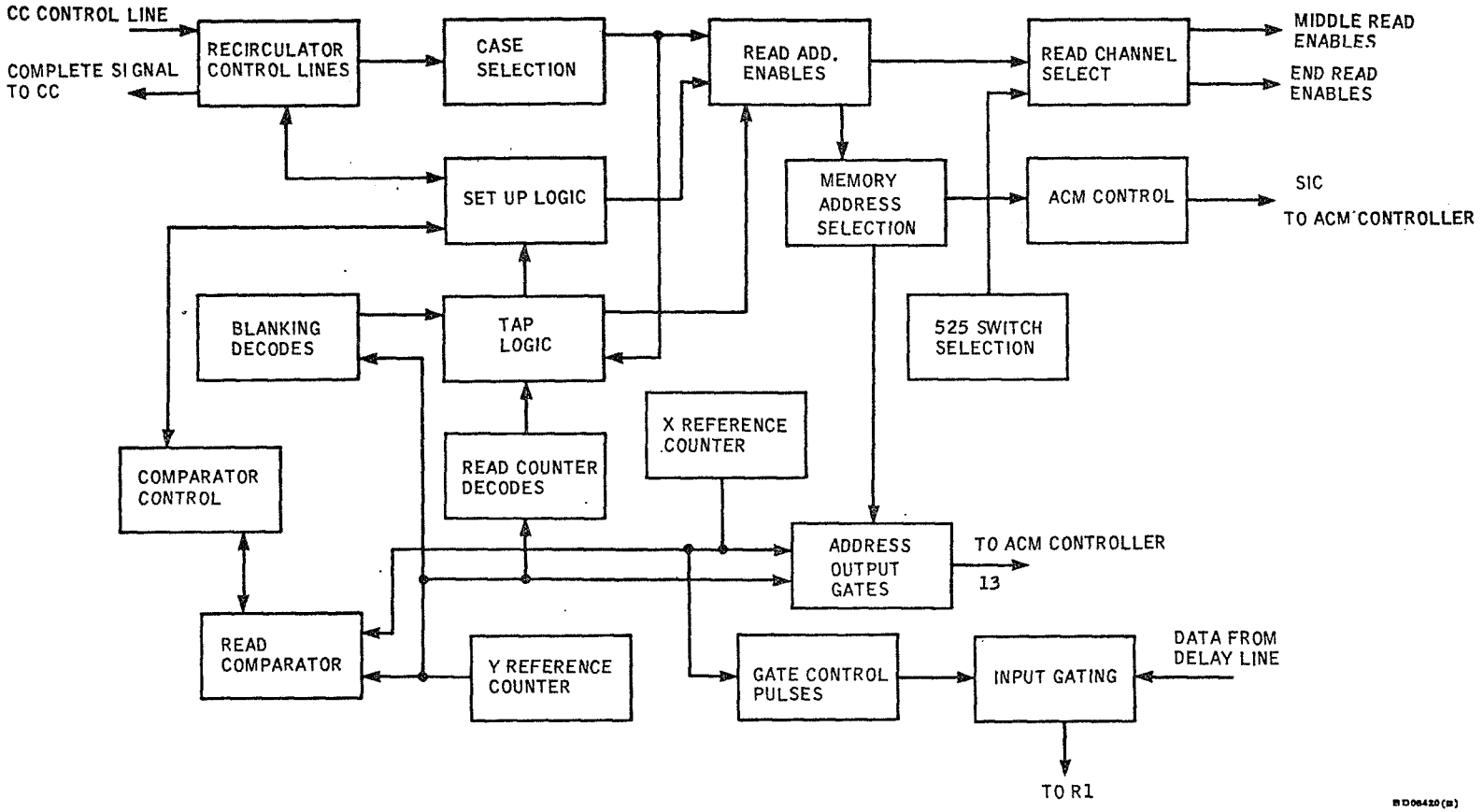

Figure 3-12 Recirculator Controller Read Cycle

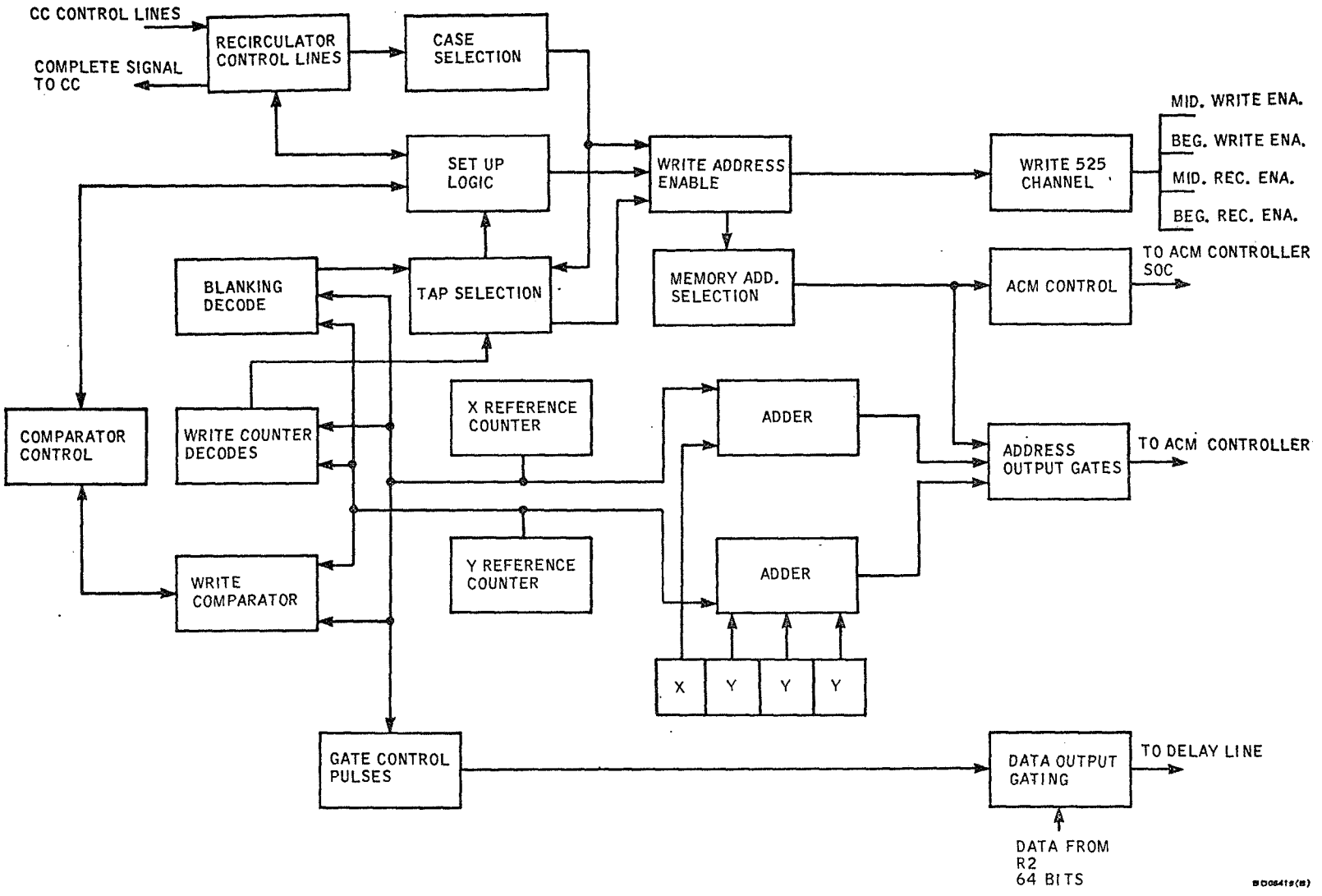

Figure 3-13 Recirculator Controller Write Cycle

10. Wait for Read Complete.

11. Reset Read Enable.

12. Reset Enable SIC FF, Read Busy, Case FF.

B. Sequence for a Write Cycle (525)

1. Let Read Complete for 525 substitute for a Write Initiate Pulse.

2. Set Write Busy FF, Lockout FF and Case FF (Write Field 1). Set Write Enable FF.

3. Set Setup FF.

4. Set Tap Selection FF.

5. Load Write Comparator, Reset Lockout FF. Enable SOC.

6. Reset Setup FF.

7. Wait for Write Complete.

8. Reset SOC Enable.

9. Reset Write Enable FF.

10. Reset cycle complete FF and Generate Write Complete Strobe Which Resets Case FF and Write Busy FF.

Let Write Complete strobe trigger another Read Initiate pulse to cause Field 2 to be read back into memory. This would be at 729 speed. Let Read Complete 2 initiate a writing sequence for 525. The second Write Complete strobe will return the DTDS to 729 operation.

C. Channel Selection. In Method I, the particular channel for display on 525 would be dialed on an octal switch. The switch output would be connected into the read channel select logic for 729 operation which would allow the contents of that particular channel to be recalled to the ACM.

The switch setting could also be connected to a compare circuit with the channel address register. When a compare is noted, new data is being sent to the assembler destined for the channel that the 525 is monitoring.

D. Tap Selection. Two things are known about the state of the operation in using this method. First, the field that has been recalled to the memory is known and second, the field of operation the 525 system is in is also known. Using this, the appropriate tap selection into the delay line can be made.

The state of the LSB flip-flop in the YERC will determine which field the 525 is in. Table 3-3 gives the correct tap selection.

3.3.2.5 Comparators

In the present DTDS, the Write and Read comparators signal the recirculator controller when a Write or Read cycle for the delay lines is complete.

Since the Read cycle from the delay line will still be at 729 rate, the read comparator will not be changed for Method I. The write comparator will operate the same and be of the same design as the 729 circuit, but will use different pulses in Method I, 525 operation.

3.3.2.6 Output Gate Control

In the 729 DTDS, various combinations of counts 8, 16, and 32 from the X Begin Write counter are used to develop the gate control pulses RMC 1, 2, 3, 4. The pulses control the flow of data from R_2 to the delay line and from the delay line to R_1. (See Figure 3-13.)

When data is being recalled to memory (from the delay line to R_1), no change is necessary in the gate control for Method I. However, new gate control pulses are needed when data is sent out for 525 display. Eight RMC pulses will control the flow of data through eight gates to the eight delay lines. The RMC pulses will be developed from counts 4, 8, 16, and 32 of the 525 X Begin Write counter.

TABLE 3-3

TAP SELECTION SEQUENCE

525 TIME	IN MEMORY	BEG. TAP	MID TAP
F2	F1	LOW	HIGH
F2	F2	HIGH	LOW
F1	F1	HIGH	LOW
F1	F2	LOW	HIGH

3.3.2.7. Serializer

In the present 729 system, data is transferred from the delay lines 16 bits at a time into the serializer which is two 8-bit shift registers. Each register is shifted by an 11.2 Mc clock. The clock arrangement is such that the output of the two registers will form an 11.2 Mc NRZ video bit stream.

In proposed Method I, the two shift registers will be operated by a 5.54 Mc clock. Each register will receive four bits from the delay line. The output of the registers will be combined to form a 5.04 Mc NRZ video bit stream for 525 display.

3.3.2.8 Delay Lines

Originally, in Method I, the 525 recirculator memory was to be patterned after the 729 system, e.g., 16 groups of four delay lines. This plan called for a 700 KC transfer clock. However, the frequency response of the delay at 700 KC is very poor. The graph, Figure 3-14, is taken from PHO-TR322, *Digital Television Display System Design Considerations*, page F-5 and shows that a much better response is available at frequencies of approximately 1.4 megacycles. By using only eight groups of four delay lines, the frequency at which data is fed into and out of the delay lines can be doubled. Hence, for any of the proposed methods that use delay lines, only 32 will be needed. This represents a substantial savings in the cost of the 525 display.

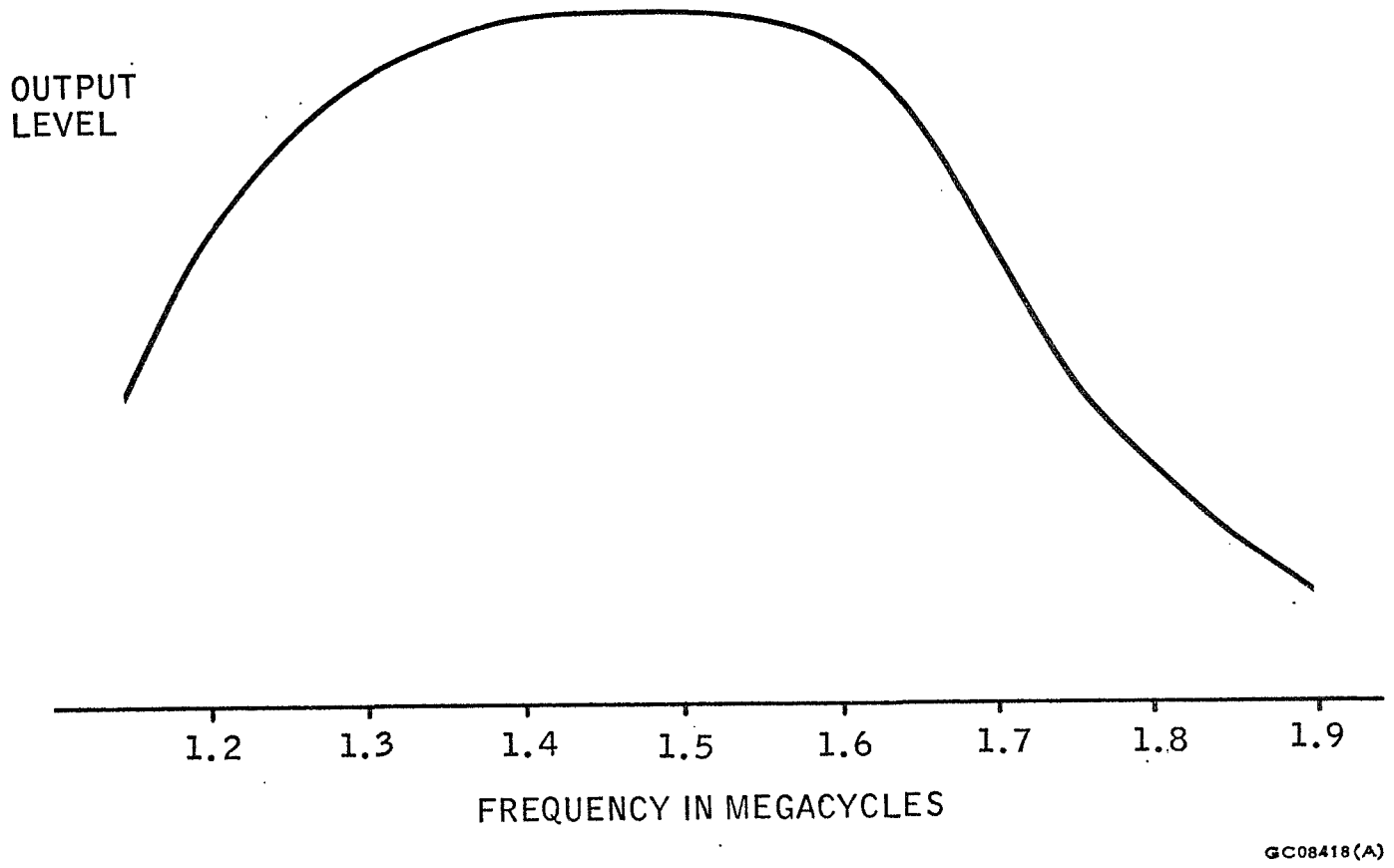

Figure 3-14 Delay Line Frequency Response

3.4 METHOD II

This method is the same as Method I except for the sequence in which 525-line DL is provided. Refer to Figure 3-15 for a typical operation. Basically, this method would write Field 1 729, write Field 1 525, write Field 2 729, and write Field 2 525. Hence, the Write cycle would be running alternately at 729 speed and 525 speed. It is readily seen that a Read/Restore memory cycle would be initiated on a Write 729 data and a Read Only cycle for 525 data. This method would eliminate Case IV and Cases VI or VII occurring together and also Case V with Case VII.

NOTE: Refer to PHO-TR323, *DCTV Final Report*, for case descriptions.

Case IV	F1DLS WRITE
CASE V	F2DLS WRITE
CASE VI	F1DLS READ
CASE VII	F2DLS READ

This means that it will take longer to update the particular 729 channel that 525 is monitoring. However, this method will generate a black and white display 33 1/3 milliseconds faster than Method I.

3.4.1 Operational Requirements

Operational requirements are the same for Method II as for Method I.

3.4.2 Modifications and/or Additions to DTDS

The modifications and/or additions will be made to those DTDS components listed in Method I, Paragraph 3.3.2. These changes will be the same as in Method I with the exceptions listed in Paragraphs 3.4.2.1 through 3.4.2.3, following.

3.4.2.1 ACM Controller

In Method II, the ACM Controller would be modified to provide control in addressing and sending readout pulses to the memory. This

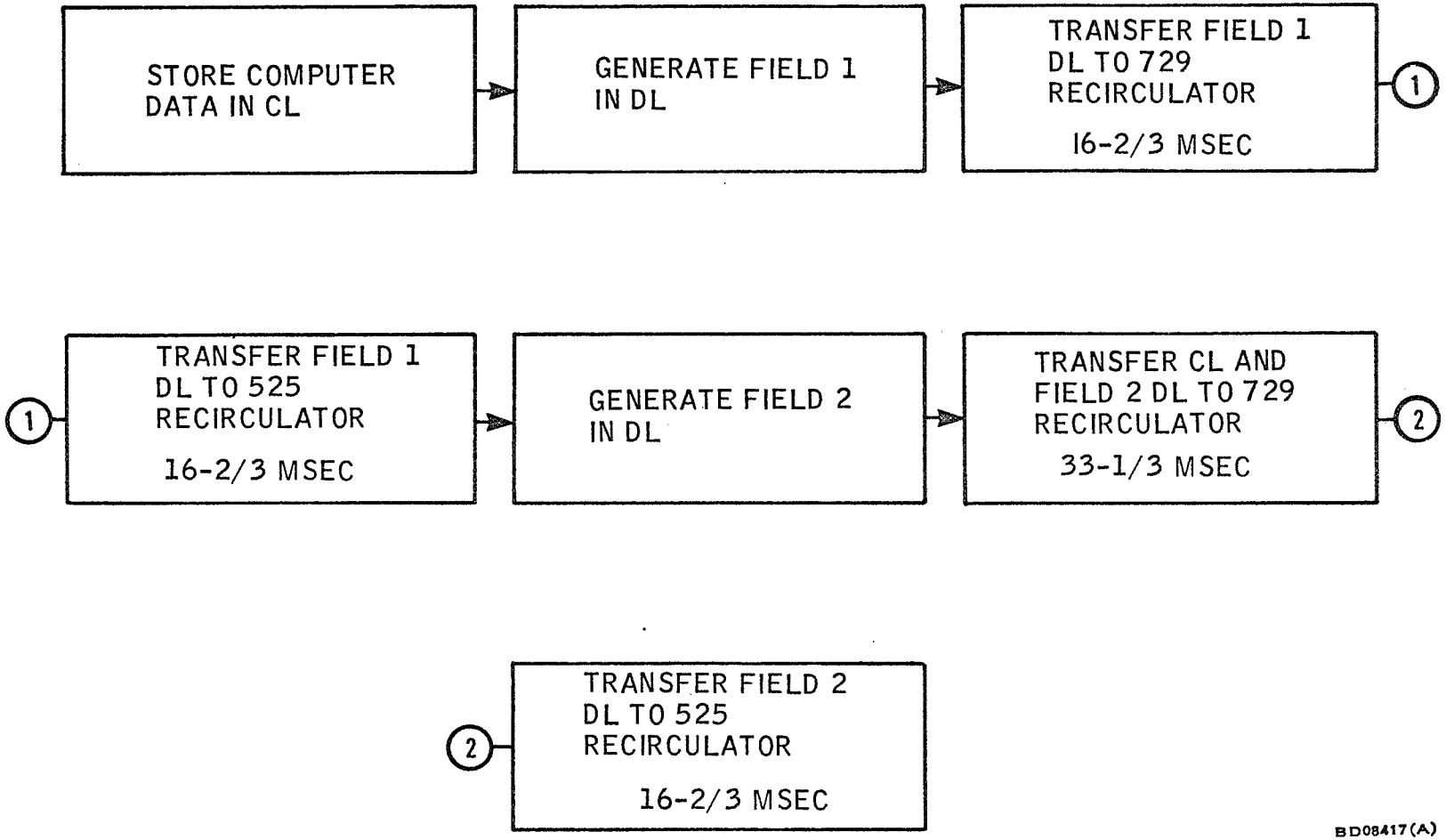

Figure 3-15 DASS B&W New Display, Method II Flow

control would provide for alternately sending 729 and 525 addresses and memory control pulses. All 525 controlling would be generated as in Method I, Paragraph 3.3.2.2.

3.4.2.2 Recirculator Controller

The controller will operate as it normally does when in a 729 Write cycle with the exceptions previously discussed. Some logic will be necessary to start the 525 Write cycle immediately after Field 1 of 729 is sent to the delay lines. The 525 Write cycle will be implemented as discussed in Method I, Paragraph 3.3.2.4. The tap selection and the channel selection would be the same as in Method I, Paragraph 3.3.2.4. Some additional control logic will be needed to prevent Cases IV or V occurring with Cases VI or VII. The recirculator controller sequence would be as follows:

A. Set up for Write to 729 delay line; select 525 display area.

B. Read/Restore memory as data is sent out to 729 delay line.

C. Write Complete 729 delay line.

D. Disable 729 control to memory, enable 525.

E. Read Only cycle for 525 data out.

F. Write Complete 525 delay line.

G. Disable 525 control to memory, enable 729.

H. Generate F2 data.

I. Read/restore memory on 729 read cycle.

J. Write complete 729 delay line.

K. Disable 729 control to memory, enable 525.

L. Read Only cycle for 525 data out.

M. Write Complete; return DTDS to 729 operation.

To initiate the above cycle, the DTDS must have all other channels and all other routines locked out. The system would be tied up for approximately 66.5 milliseconds for a black and white display.

3.4.2.3 New Data

When an update is decoded for 729 data, both CL and F1 DL are recalled to the memory. The new data is then generated and is used to replace the old. In this method, either one or two approaches could be used to display 525 data. Field 1 of new data could circulate with Field 2 old data for one frame, or, at the time Field 1 new data is written on the delay line, Field 2 old data could be destroyed. In the latter approach, Field 1 data could circulate alone in the delay line for one frame time.

3.5 METHOD III

This method is a single channel operation as opposed to the dual channel operations called out in the other methods. Both CL and DL are stored on the 525 recirculator memories (RM). However, as with the other methods, if the CL is not restricted to the addressing, as discussed earlier, all the DL generated by the Display Assembler Subsystem (DASS) will not be placed on the 525 RM. If, on the other hand, the CL is restricted, then the 525 channel will operate the same as the present 729 channels. Refer to Figure 3-17 for Method III DASS block diagram.

The storage capacity for CL, for this method, is reduced from 3072 words to 1455 words. By addition of extra circuits and delay lines, the 1455 CL word storage could be doubled.

3.5.1 Operational Characteristics

This method would operate the same as a 729 operation except for the addressing restriction. Refer to Figure 3-16 for a typical operation sequence.

3.5.2 Modifications and/or Additions to DTDS

The following modifications and/or additions to the DTDS components will be necessary for Method III implementation:

A. New Clock Systems

B. X and Y Reference Counters

C. Sync Pulse Generator

D. CL Reference Counters

E. CL Address Reference Counter

F. Recirculator Controller

G. Comparators

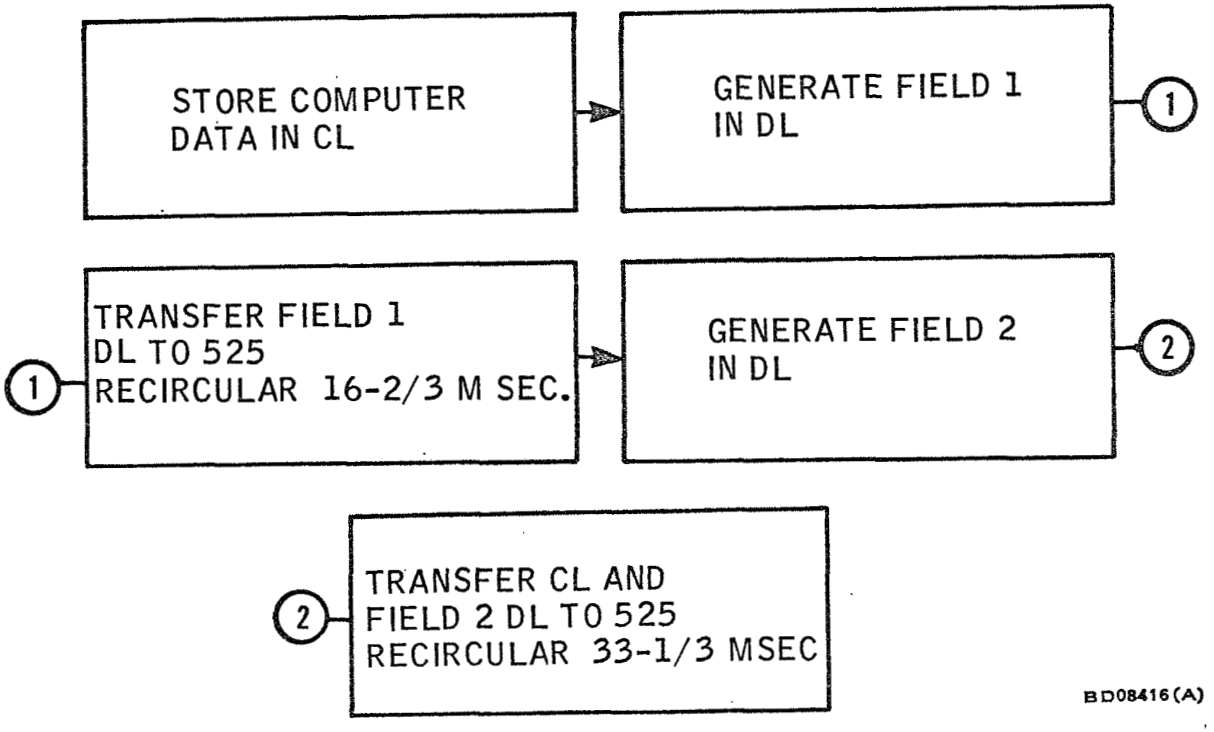

Figure 3-16 DASS B&W New Display, Method III Flow

H. Read Counter Decode

I. Write Counter Decode

J. Blanking Decode

K. ACM Controller

L. Display Area.

M. Output Gating

N. Delay Lines

O. Serializer.

The changes and new circuits not previously discussed in the other methods will be discussed in further detail.

3.5.2.1 CL Counters

In this proposed method, provisions must be made to store computer language. To do this in 729 operation requires four CL counters and a CLS address register. The four CL counters, CL End Read, CL Middle Read, CL Middle Write, and CL Begin Write, will be required for 525 operation. These counters are associated with the corresponding Y reference counters. The count in the registers is decoded octally, and the maximum decode is 17777, which corresponds to the last of the 3072 addresses in CL storage. For 525, Method III, the counters would operate as they do for 729 except that the maximum count would be 14656_8, which corresponds to 1455 CL addresses.

3.5.2.2 CL Address Register (CLAR)

In 729, the CLAR is used to address computer language words in the CL portion of the ACM. It would perform the same function in 525.

3.5.2.3 Recirculator Controller

Since the 525 will be operating independently, data must travel both to and from the delay line. Consequently, the recirculator controller must operate entirely at 525 speed. The controller would be constructed identically to the one presently operating in the DTDS system. See page 3-56 of PHO-TR323, *DCTV Final Report*, for an explanation of its functions.

3.5.2.4 Comparators

In the present DTDS, both the Read and Write comparators notify the recirculator controller when a Read or Write cycle to the recirculator memory is complete. The 525 circuits would be constructed identical to the 729 logic, but they would use different pulses.

3.5.2.5 Read, Write, and Blanking Decodes

All three of these decoding circuits furnish control pulses to the tap selection logic. Since the length of time of operation for each of these will differ from 729, they must all be designed to perform the same functions, but at a slower speed.

3.5.2.6 ACM Controller

The ACM controller would act just as it does in 729 operation except that it would be at 525 timing. For an explanation of its functions, refer to PHO-TR323, *DCTV Final Report*, page 3-73.

3.5.2.7 Display Area

In this method, a fixed display would be used. Thus, either one of the four corner areas or the center area of a 729 frame would be chosen. The fixed display approach is discussed in Method I, Paragraph 3.3.2.2.

3.6 METHOD IV

This method would involve the addition of essentially a 525-line video display assembler subsystem (DASS/525). The DASS/525 would operate in a slave mode from the DTDS and would contain a core memory, X and Y counters, sync generator, delay lines, and the necessary control circuitry. Although it is called a display assembler, it contains no symbol generator and other circuitry necessary to generate DL from CL. The DASS/525 would merely take the already-processed DL and output a portion at a 525-line video rate.

In this method, as in Method I, no provision was made to have the 525 channel operate alone. These methods provide only for storing a portion of DL on the 525 RM, with the CL and the total DL being stored on a 729 RM. Since this method calls for no modification to the existing DTDS other than possible addition of line drivers to provide the necessary control signals needed by the DASS/525, it is felt that the "Dual Channel" concept is best.

However, if desired, a single channel with 525-line video could be provided. This would call for an increased core size, additional control circuitry, and some modification to the DTDS. Approximately 1455 CL words could be stored on the 525 RM. It should also be noted that this method calls for both a core and a recirculator memory. These were provided so that flicker would not appear on the 525-line video when the core was being updated. If this flicker would not be objectional, the core could provide the 525-line video. When being updated, the core would have to stop refreshing the video line for approximately one frame time. (See Figures 3-17 and 3-18.)

3.6.1 Operational Requirements

This method would impose no changes on the present DTDS operational procedures other than the previously mentioned addressing restrictions. It would only require the operator to select the channel for 525-line presentation and to select the 525 mode. Refer to Figure 3-19 for the information flow for a typical DTDS Method IV operation.

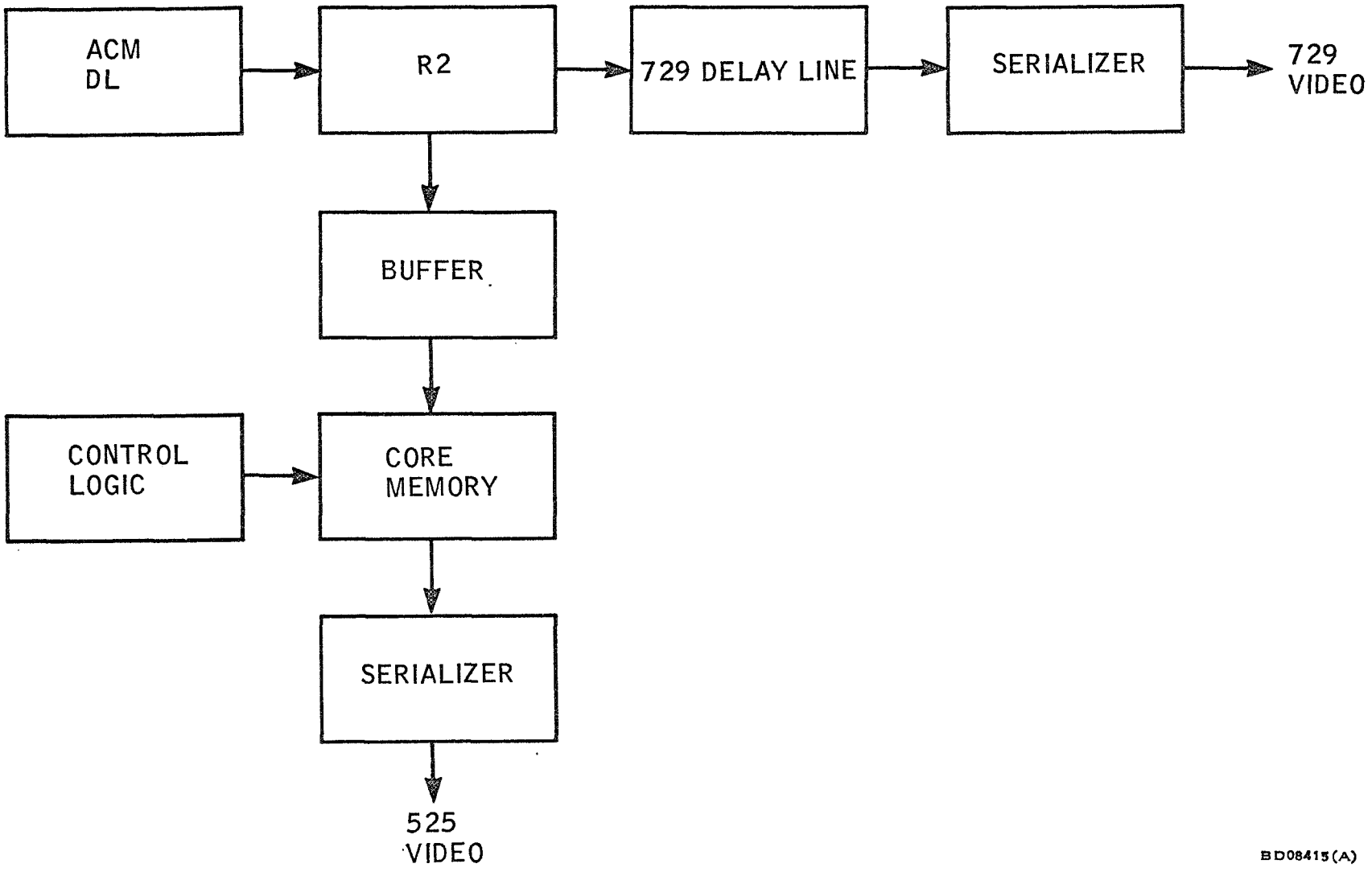

Figure 3-17 Method II Block Diagram, Without Recirculator

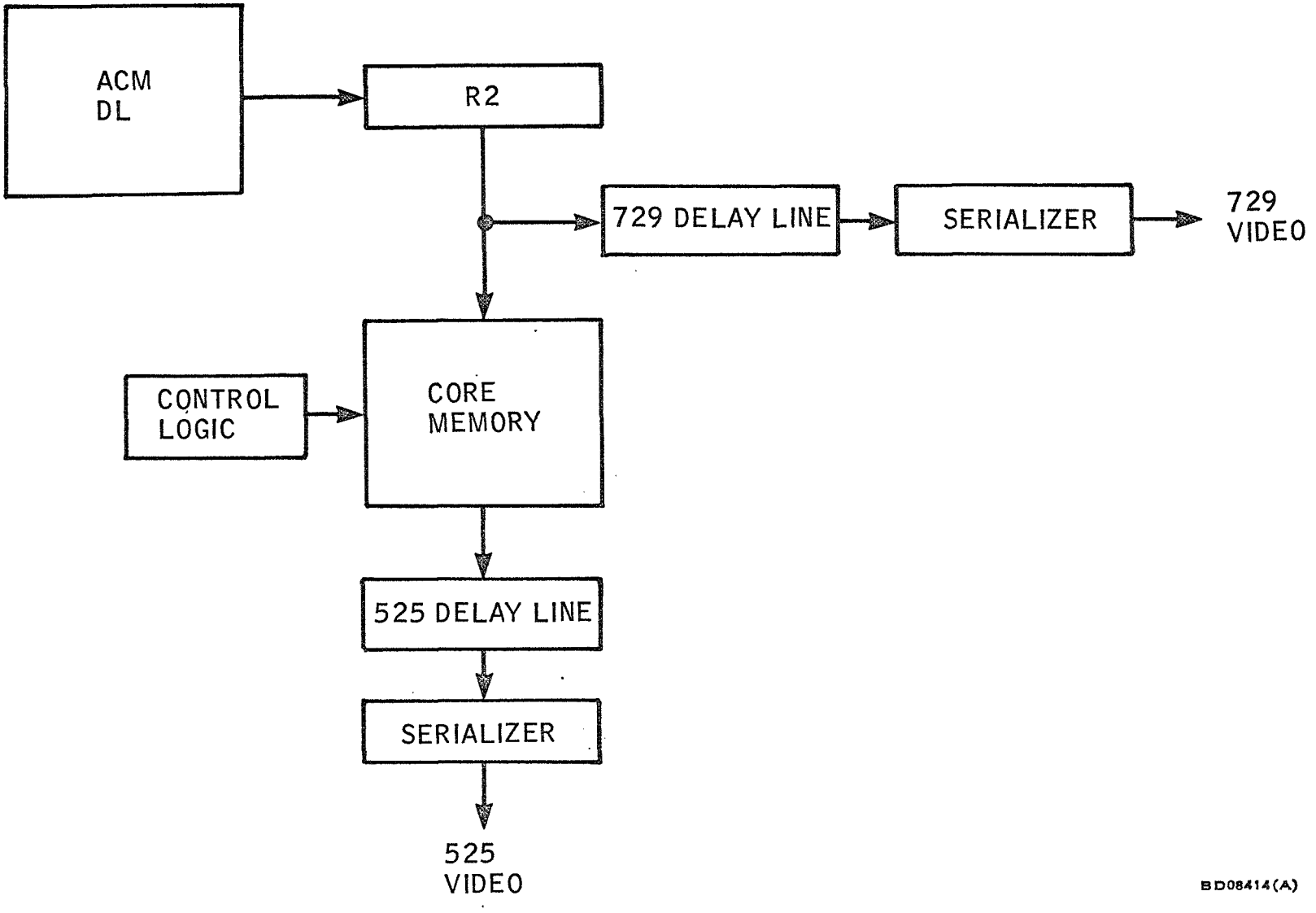

Figure 3-18 Method II Block Diagram, With Recirculator

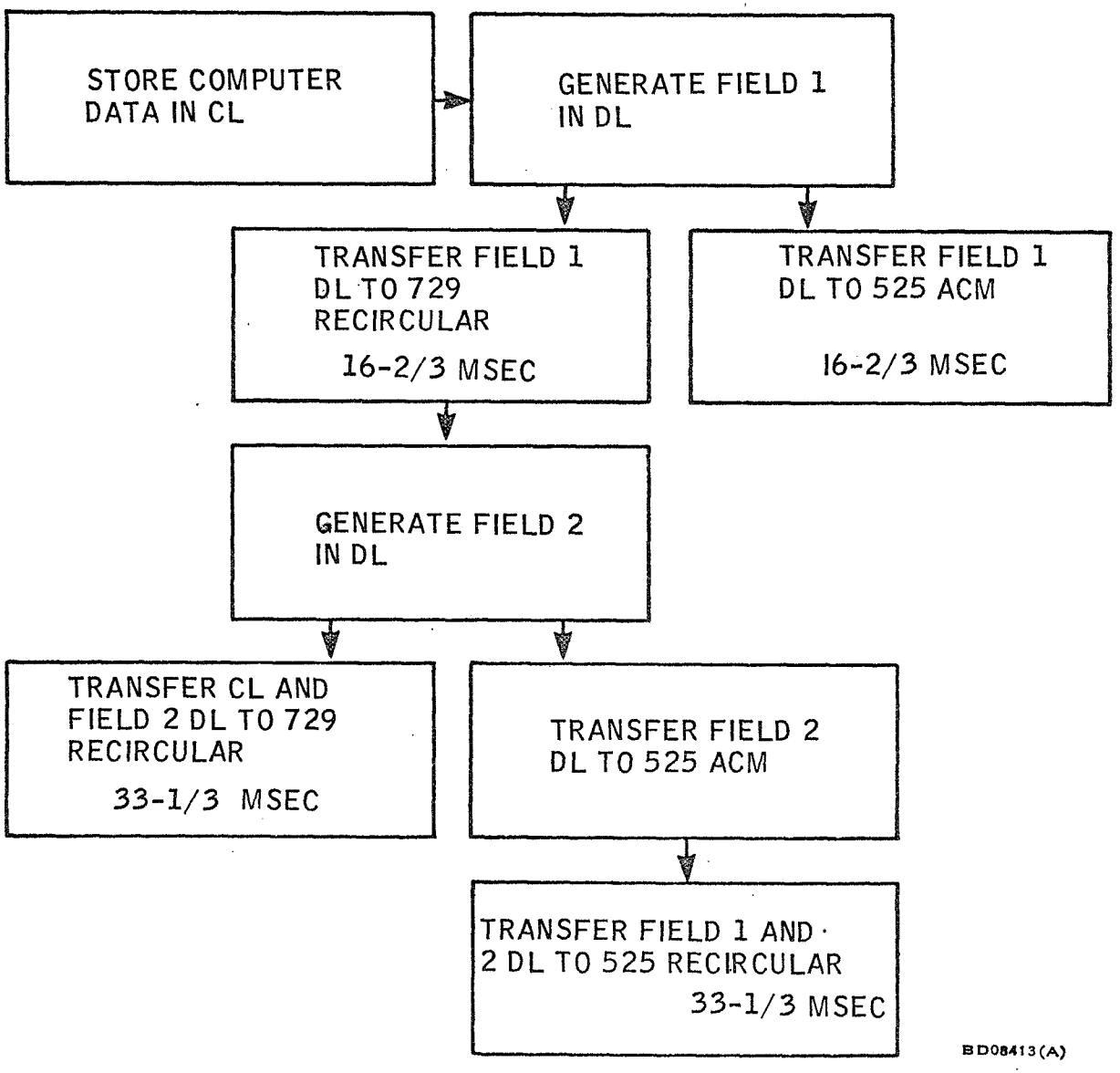

Figure 3-19 DASS B&W New Display, Method IV Flow

3.6.2 DASS/525 Components

The following DASS/525 components will be required to implement Method II.

A. New oscillator timing

B. X and Y reference counters

C. Sync pulse generator

D. Memory controller

   1. Addressing

   2. Write-In and Readout pulses

E. Display area control

F. Recirculator control

   1. Tap selection

   2. Channel selection

   3. New data

G. Comparator

H. Data output gating

I. Serializer

J. Delay lines

K. Core memory

L. Buffer.

3.6.2.1 Component Changes Similar to Method I

The oscillator timing, X and Y reference counters, comparator, sync pulse generator, and serializer will be the same as discussed for Method I. If delay lines are used in this method, the recirculator controller Write cycle and data output gating will be the same as for Method I.

3.6.2.2 Memory Control

Using delay lines the memory control would function just as the ACM controller does in 729 operation. (The addressing to the memory will be discussed under Display Control, Paragraph 3.6 2.3.) The SIC and SOC pulses to the memory would be limited to nine per line and controlled as described in Method I, Paragraph 3.3.2.2. The buffer circuit would not be needed in this variation. If delay lines are not used, the controller would develop the SOC pulses in such a manner that the DL characters would be sent to the serializer every 33.4 msec. A Read/Restore cycle would be initiated each time until new data was sensed at the buffer. At this time, the new data would be written in with a Clear Write mode.

3.6.2.3 Display Control

A. Fixed. The desired area to be displayed in 525 could be fixed to the upper left, lower left, or center portion of the 729 display. The 525 addressing would be connected in such a manner as to give the desired area given above.

B. Variable. The variable control will allow any portion of the 729 picture to be displayed. This variable control differs from the type discussed in Method I. (See Figure 3-20.) The output addressing is the variable in Method I, whereas in this method the input addressing is the variable. Since the cost is important, the size of the memory should be as small as possible. Consequently, the 525 display size is selected.

   The operator would set the starting address on some switches whose output is compared to the 729 memory addressing. When the desired address is reached, as determined by the compare

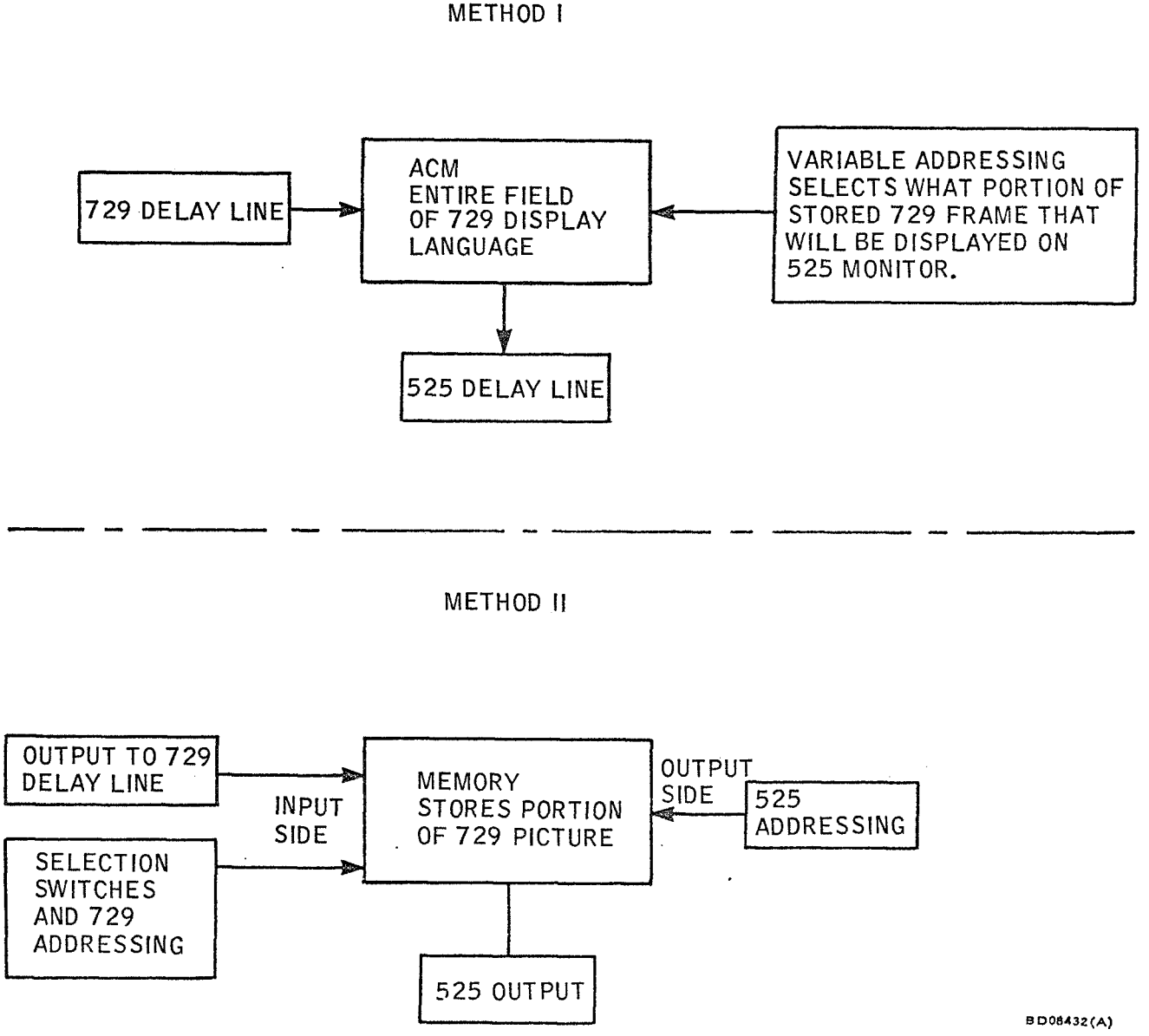

Figure 3-20 Comparison of Variable Addressing

signal, addressing to the new memory would start. The data being sent out to the 729 delay line would then be stored in the memory. Upon receipt of a Write Complete, as determined by a 525 Write comparator (both fields), the 525 addressing to the memory would become active, and the data could be transferred out to the 525 monitor. The variable control, although requiring more logic to implement than the fixed display, does give the operator a degree of freedom in selecting the viewing area. It should be noted that the area to be displayed in 525 must be selected before the data is presented for viewing in 729.

3.6.2.4 Recirculator Control

If the delay lines are not used, there is no need for the recirculator controller. However, if the delay lines are used, the controller would function as described in Method I, Paragraph 3.3.2.4. Handling of new data would be as follows:

Anytime new data is sent out to the 729 display, the 525 display would be disabled. This is necessary because the memory cannot be read from and written into at the same time. Thus the 525 display would be off for approximately 33 milliseconds while the memory is being updated. The result would be a blink in the picture while new data is fed in. This blinking could be avoided on updating if delay lines were used. In this case updating would occur as it does in 729 operation.

3.6.2.5 Buffer

The buffer would be between the 729 output gating and the input to the memory. The 64-bit stage would not be used if delay lines are employed.

SECTION 4

COMPARISON OF METHODS

4.1 GENERAL

The proposed methods are compared in the following major categories:

- DTDS downtime for modification
- Cost
- Changes in present operation characteristics
- Modifications to DTDS.

As can be expected, no one method possesses the most desirable rating in every category.

4.2 DTDS DOWNTIME FOR MODIFICATION

Methods I, II and III will require considerable time for DTDS modification. The DTDS will be down due to the need for extensive rewiring in the DASS. Method IV would require little or no DTDS downtime since the only possible changes would consist of the addition of line drivers to the existing system.

4.3 COST

The cost of any one of the first three methods is directly related to the amount of rewiring and addition of logic modules required. Methods I and II would be the least costly methods. Because of the more complicated control functions, Method III implementation would cost more than the first two methods. Method IV is the most expensive as it would require essentially all the circuitry of Method I with the addition of a core memory and memory control circuitry.

4.4 CHANGES IN PRESENT OPERATIONAL CHARACTERISTICS

All the methods impose the same restriction on the operating procedures. These restrictions concern addressing, as pointed out previously.

The differences on the update rates for the different methods are as follows:

- Method I - Adds 66 2/3 msec to existing rate
- Method II - Adds 33 1/3 msec to existing rate
- Method III - No change in rate
- Method IV - No change in rate.

4.5 MODIFICATIONS TO DTDS

Methods I, II, and III require major modifications to the DTDS Display Assembler. The required additional logic needed will probably require the addition of racks since unused space in the existing racks is limited. Method IV will require only minor modifications to the DTDS but will require a rack (two if delay lines are used) for the additional logic and core memory. Table 4-1 depicts these comparisons.

TABLE 4-1

METHOD COMPARISON

	METHOD I	METHOD II	METHOD III	METHOD IV
DTDS MOD. DOWNTIME	MEDIUM	MEDIUM	LONG	SHORT
COST	LEAST	LEAST	MEDIUM	MOST
TIME ADDED TO UPDATE RATES	66 2/3 MSEC	33 1/3 MSEC	0	0
DTDS MODIFICATIONS	MAJOR	MAJOR	MAJOR	MINOR

SECTION 5

SUMMARY

5.1 METHODS I AND II

These methods are dual channel in nature, with 729-line DL and CL placed on a 729-line recirculator memory. A portion of 729-line DL is then placed on a 525-line recirculator memory. These two methods differ only in the sequence in which the DL for the 525-line video is obtained. These methods require the following:

- 525-line recirculator memory
- 525 sync and timing circuitry
- Additional counters and control circuitry.

5.2 METHOD III

This method utilizes a single channel with both CL and DL stored on the 525-line recirculator memory. The CL will be processed the same as any 729-line CL, but only that portion of DL within the intervals of $0 \leq x \leq 576$, $0 \leq y \leq 480$ (Display Coordinates) will be put on the 525-line recirculator memory. Also, the storage of CL words is limited to 1455 words. This method would require the circuitry required for Methods I and II, with the counters and control circuitry being more complex.

5.3 METHOD IV

This method is also a dual channel mode of operation with the 525-line converter placed external to the DTDS. Whenever DL is transferred from the DTDS ACM to the DTDS RM, the 525 converter extracts a portion of this DL from the data transfer bus and stores it in a core memory. Upon completion of the data transfer, this DL is then transferred to the 525-line recirculator memory. This method requires the following:

- 525-line sync and timing
- 525-line recirculator memory
- Core memory
- Counters and control circuitry.

SECTION 6

RECOMMENDATIONS

6.1 GENERAL

Method IV is recommended for implementation for the following reasons:

A. DTDS will be inoperative for the least amount of time

B. Least risk factor is involved since DTDS modifications are minor

C. Method would be adaptable for conversion of other digital television systems' video.

Method I would be recommended for implementation, since it involves lower cost and the least amount of time to implement, if the DTDS could be made available for several months for modification. However, one of the ground rules was that the DTDS downtime should be minimized.

Method II and Method III are not recommended since they involve extensive modifications to the DTDS. It is not felt that the faster data generation times of these two methods over that of Method I are sufficient to qualify their selection.